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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,408	12/29/2000	Paolo Faraboschi	00-BN-057 (STMI01-00057)	7821

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/751,408	FARABOSCHI ET AL.
	Examiner	Art Unit
	Eric Coleman	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7,8,9-14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (patent No. 6,282,633) in view of Tran (patent No. 6,006,324) and Poland (patent No. 6,173,305).

3. Killian taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Instruction execution pipeline with N processing stages (e.g., see fig.2);

b) Means to fetch into the instruction pipeline from the instruction cache (e.g., see fig. 2 and col. 4, lines 41-56);

b) Constant generator unit capable of receiving the fetched instruction syllables and capable of generating at least one constant operand by decoding the at least one operand instruction comprising at least one syllable containing K-bit constant field containing k-bits that represent a constant operand (e.g., see col. 5, lines 52-63)..

4. Killian did not expressly detail (claim 1) that the constant generator performing at least one of: right justifying the K bits to produce a short constant operand (e.g., see col. 73, lines 11-66), and combining the K bits with T bits of data form a T bit constant field

to produce a long constant operand. Poland, however, taught a data unit that provided this operation (e.g., and col. 71, line 6-col. 72, line 64).

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Killian and Poland the incorporation of the data functions of the Poland data unit of at least right justifying and masking the operand would have allowed the Killian to extract operand constants quickly (e.g., see col. col. 71,line 6-col. 72,line 64).

6. Killian did not expressly detail (claim 1) that the means to fetch instructions to the pipeline comprised an instruction issue unit. Tran however taught use of issue units to fetch instructions from the cache and issue to execution pipelines (e.g., see figs. 10,36 and col. 8, line 36-col. 10, line 59).

7. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Killian and Tran. The addition of the parallel issue of the instructions from the cache would have allowed the Killian system to provide increased throughput in fetching decoding and processing the instructions from cache. Therefore one of ordinary skill in the DP art would have been motivated to use the parallel issue units of Tran at least to increase the throughput of the system.

8. As per claim 2, Killian taught the syllable contained at least one opcode field that contained at least one opcode (e.g., see col. 5, lines 52-63 and col. 9, lines 29-46).

9. As per claims 3,4,5 Killian taught an input data path coupled to a sign extension unit, the input data path capable of providing to the sign extension unit K-bits of data that represent a short constant operand within the at least one syllable; wherein the sign extension unit is capable of right justifying the K-bits of data in an output syllable and

zero-extending (I8UI, L16UI) or one-extending (L16SI) the K-bits; and an output data path coupled to the sign extension unit capable of receiving from the sign extension unit the output syllable containing justified K-bits of data that represent the short constant operand (e.g., see fig. 1d and col. 7, lines 1-56) Poland also taught these limitations (e.g., see col. 71, line 6-col. 74, line 67).

10. As per claim 6, Killian taught constant instructions with plural constant fields comprising high order bits and low order bits (e.g., see col. 9, lines 19-62 and col. 13, line 15-col. 14, line 36).

11. As per claims 7,11,14, Killian taught instruction formats of 32 bits with various combinations of numbers of bits for the high and low order bits. (e.g., see col. 13, lines 15-65). Therefore although Killian did not specify the combination of 9 bit field and a 23 bit field one of ordinary skill would have been motivated to incorporate an instruction with a 9 bit field and a 23 bit field in order to provide a 32 bit field as taught by Killian depending on the number of instructions were to be used in the system which would have corresponded to the number of bits in the opcode field before sign extension.

12. As per claim 8,9 Tran taught multiplexers controlled by multiplexer control circuit using predecode tags for determining which path to select and whether the constant operand instruction is to decode a long constant operand (e.g. see figs. 3, 4a, 4c and col. 8, line 47-col. 13, line 40).

13. As per claim 10, Killian taught plural input paths for instructions to multiplexers and output path for each multiplexer where the input paths received instructions with

constant operands and the constant portions were combined (e.g., see col. 5, line 52-col. 6, line 24).

14. As per claim 12,13, Killian did not specifically detail the constant generator enabling the first and second bit of the multiplexer depending on predetermined bits (EXT bits). Tran however, taught multiplexer with input for receiving a syllable from a first issue lane and another syllable from a second issue lane and coupled to an output path for sending to the output path, one of the bits from the first issue lane and the second lane and constant generator for enabling the inputs to the multiplexer depending on comparison with predetermined numbers (e.g., see fig. 3, and col. 8, line 53-col. 13, line 40).

15. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Killian and Tran. The addition of the parallel issue of the instructions from the cache would have allowed the Killian system to provide increased throughput in fetching decoding and processing the instructions from cache. Therefore one of ordinary skill in the DP art would have been motivated to use the parallel issue units of Tran at least to increase the throughput of the system.

16. Claims 15-18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (patent No. 6,282,633) in view of Poland (patent No. 6,173,305).

17. Killian taught the invention as claimed including a data processing ("DP") system comprising:

a) Instruction execution pipeline with N processing stages (e.g., see fig.2);

b) Means to fetch into the instruction pipeline from the instruction cache (e.g., see fig. 2 and col. 4, lines 41-56);

b) Constant generator unit capable of receiving the fetched instruction syllables and capable of generating at least one constant operand by decoding the at least one operand instruction comprising at least one syllable containing K-bit constant field containing k-bits that represent a constant operand (e.g., see col. 5, lines 52-63).

18. Further as per claims 15,16,17,18, Killian taught an input data path coupled to a sign extension unit, the input data path capable of providing to the sign extension unit K-bits of data that represent a short constant operand within the at least one syllable; wherein the sign extension unit is capable of right justifying the K-bits of data in an output syllable and zero-extending (I8UI, L16UI) or one-extending (L16SI) the K-bits; and an output data path coupled to the sign extension unit capable of receiving from the sign extension unit the output syllable containing justified K-bits of data that represent the short constant operand (e.g., see fig. 1d and col. 7, lines 1-56).
As to the "capable of ..." limitations these limitations are not positively recited and therefore these limitations only require the "ability" of the prior art to perform the limitations. Here the Killian reference has the elements that have the ability to perform these limitations.

19. On the other hand Poland taught (claim 15-18) that the data unit performing sign extension of a K-bit operand that represented a short operand within a syllable and right justifying the K-bits of data in an output syllable and zero extending or one extending

the K-bits and an output data path (e.g., see col. 73, lines 1-66), and (e.g., and col. 71, line 6-col. 72, line 64).

20. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Killian and Poland the incorporation of the data functions of the Poland data unit of at least right justifying and masking the operand would have allowed the Killian to extract operand constants quickly (e.g., see col. col. 71,line 6-col. 72,line 64).

21. As to the long constant limitation of claim 18, Killian taught encoding various lengths of operands (long and short) (e.g., see col. 9, lines 10-62).

Claim Rejections - 35 USC § 103

22. Claims 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (patent No. 6,282,633) in view of Poland (patent No. 6,173,305).

23. Killian taught the invention as substantially as claimed including a data processing ("DP") system comprising:

a) Instruction execution pipeline with N processing stages (e.g., see fig.2);

b) Means to fetch into the instruction pipeline from the instruction cache (e.g., see fig. 2 and col. 4, lines 41-56);

b) Constant generator unit capable of receiving the fetched instruction syllables and capable of generating at least one constant operand by decoding the at least one operand instruction comprising at least one syllable containing K-bit constant field containing k-bits that represent a constant operand (e.g., see col. 5, lines 52-63).

24. Further as per claims 15,16,17,18, Killian taught an input data path coupled to a sign extension unit, the input data path capable of providing to the sign extension unit K-bits of data that represent a short constant operand within the at least one syllable; wherein the sign extension unit is capable of right justifying the K-bits of data in an output syllable and zero-extending (I8UI, L16UI) or one-extending (L16SI) the K-bits; and an output data path coupled to the sign extension unit capable of receiving from the sign extension unit the output syllable containing justified K-bits of data that represent the short constant operand (e.g., see fig. 1d and col. 7, lines 1-56).

As to the "capable of ..." limitations these limitations are not positively recited and therefore these limitations only require the "ability" of the prior art to perform the limitations. Here the Killian reference has the elements that have the ability to perform these limitations.

25. On the other hand Poland taught (claims 15-18) that the data unit performing sign extension of a K-bit operand that represented a short operand within a syllable and right justifying the K-bits of data in an output syllable and zero extending or one extending the K-bits and an output data path (e.g., see col. 73, lines 1-66), and (e.g., and col. 71, line 6-col. 72, line 64).

26. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Killian and Poland the incorporation of the data functions of the Poland data unit of at least right justifying and masking the operand would have allowed the Killian to extract operand constants quickly (e.g., see col. col. 71,line 6-col. 72,line 64).

27. As to the long constant limitation of claim 18, Killian taught encoding various lengths of operands (long and short) (e.g., see col. 9, lines 10-62).

28. As per claim 19 Killian taught instruction formats of 32 bits with various combinations of numbers of bits for the high and low order bits. (e.g., see col. 13, lines 15-65). Therefore although Killian did not specify the combination of 9 bit field and a 23 bit field one of ordinary skill would have been motivated to incorporate a instruction with a 9 bit field and a 23 bit field in order to provide a 32 bit field as taught by Killian depending on the number of instructions were to be used in the system which would have corresponded to the number of bits in the opcode field before sign extension.

29. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Poland as applied to claim 18,19 above, and further in view of Tran (patent No.6,006,324).

30. Killian did not specifically detail the constant generator enabling the first and second bit of the multiplexer depending on predetermined bits (EXT bits). Tran however, taught multiplexer with input for receiving a syllable from a first issue lane and another syllable from a second issue lane and coupled to an output path for sending to the output path one of the bits from the first issue lane and the second lane and constant generator for enabling the inputs to the multiplexer depending on comparison with predetermined numbers (e.g., see fig. 3, and col. 8, line 53-col. 13, line 40).

31. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Killian and Tran. The addition of the parallel issue of the instructions from

the cache would have allowed the Killian system to provide increased throughput in fetching decoding and processing the instructions from cache. Therefore one of ordinary skill in the DP art would have been motivated to use the parallel issue units of Tran at least to increase the throughput of the system.

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kregness (patent No. 4,595,911) disclosed a programmable reformat system (e.g., see abstract).

England (patent No. 4,109,310) disclosed a variable field length addressing system having data byte interchange (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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EC

ERIC COLEMAN
PRIMARY EXAMINER